Revision History

Revision 0.1 (Oct. 2007)
- Preliminary release.

Revision 0.2 (Mar. 2008)..
- Modify package thickness spec from 1.2mm to 1.4mm.
- add 166/333Mhz @CL3 speed.

Revision 0.3 (Oct. 2008)..
- Modify package thickness to 1.2mm..
- Improve ICCs spec.

Revision 0.4 (Feb. 2009)..
- Release. (none Preliminary)

1Gb (8M·4Bank·32) Double DATA RATE SDRAM

Features

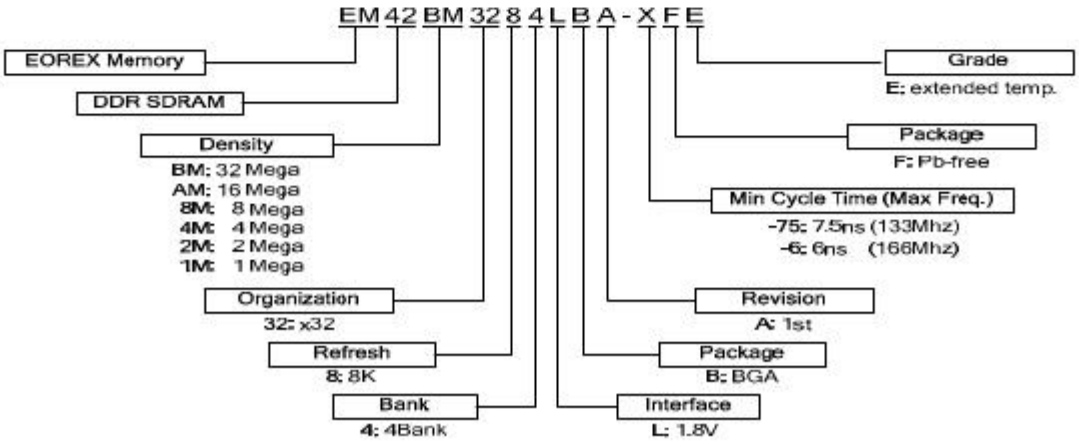
- Internal Double-Date-Rate architecture with 2 Accesses per clock cycle.
- 1.8V ±0.1V VDD/VDDQ
- 1.8V LV-COMS compatible I/O
- Burst Length (B/L) of 2, 4, 8, 16
- 3 Clock read latency
- Bi-directional,intermittent data strobe(DQS)
- All inputs except data and DM are sampled at the positive edge of the system clock.
- Data Mask (DM) for write data
- Sequential & Interleaved Burst type available
- Auto Precharge option for each burst accesses
- DQS edge-aligned with data for Read cycles
- DQS center-aligned with data for Write cycles
- No DLL ;CK to DQS is not synchronized
- Deep power down mode
- Partial Array Self-Refresh(PASR)
- Auto Temperature Compensated Self-Refresh (TCSR) by built-in temperature sensor
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms

Description

The EM42BM3284LBA is Double-Date-Rate Synchronous DRAM fabricated with ultra high performance CMOS process containing 1,073,741,824 bits which organized as 8Meg words x 4 banks by 32 bits.
The 1Gb DDR SDRAM uses a double data rate architecture to accomplish high-speed operation.
The data path internally pre-fetches multiple bits and It transfers the data for both rising and falling edges of the system clock. It means the doubled data bandwidth can be achieved at the I/O pins.
Available packages:TFBGA-90B(13mmx11mm).

Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM42BM3284LBA-6F	32M X 32	166MHz/DDR333 @CL3	TFBGA-90B	Commercial	Free
EM42BM3284LBA-75F	32M X 32	133MHz/DDR266 @CL3	TFBGA-90B	Commercial	Free



* EOREX reserves the right to change products or specification without notice.

Pin Assignment

1	2	3		7	8	9
VSS	DQ31	VSSQ	A	VDDQ	DQ16	VDD
VDDQ	DQ29	DQ30	B	DQ17	DQ18	VSSQ
VSSQ	DQ27	DQ28	C	DQ19	DQ20	VDDQ
VDDQ	DQ25	DQ26	D	DQ21	DQ22	VSSQ
VSSQ	DQS3	DQ24	E	DQ23	DQS2	VDDQ
VDD	DM3	NC	F	NC	DM2	VSS
CKE	CLK	/CLK	G	/WE	/CAS	/RAS
A9	A11	A12	H	/CS	BA0	BA1
A6	A7	A8	J	A10	A0	A1
A4	DM1	A5	K	A2	DM0	A3
VSSQ	DQS1	DQ8	L	DQ7	DQS0	VDDQ
VDDQ	DQ9	DQ10	M	DQ5	DQ6	VSSQ
VSSQ	DQ11	DQ12	N	DQ3	DQ4	VDDQ
VDDQ	DQ13	DQ14	P	DQ1	DQ2	VSSQ
VSS	DQ15	VSSQ	R	VDDQ	DQ0	VDD

90ball TFBGA / (13mm x 9mm x 1.2mm)

Pin Description (Simplified)

Pin	Name	Function
G2,G3	CLK,/CLK	**(System Clock)** Clock input active on the Positive rising edge except for DQ and DM are active on both edge of the DQS. CLK and /CLK are differential clock inputs.
H7	/CS	**(Chip Select)** /CS enables the command decoder when ”L” and disable the command decoder when “H”.The new command are over-Looked when the command decoder is disabled but previous operation will still continue.
G1	CKE	**(Clock Enable)** Activates the CLK when “H” and deactivates when “L”. When deactivate the clock,CKE low signifies the power down or self refresh mode.
J8,J9,K7,K9,K1, K3,J1~J3,H1~H3,	A0~12	**(Address)** Row address (A0 to A12) and Calumn address (CA0 to CA9) are multiplexed on the same pin. CA10 defines auto precharge at Calumn address.
H8,H9	BA0, BA1	**(Bank Address)** Selects which bank is to be active.
G9	/RAS	**(Row Address Strobe)** Latches Row Addresses on the positive rising edge of the CLK with /RAS “L”. Enables row access & pre-charge.
G8	/CAS	**(Column Address Strobe)** Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
G7	/WE	**(Write Enable)** Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
L8,L2,E8,E2	DQS0~3	**(Data Input/Output)** Data Inputs and Outputs are synchronized with both edge of DQS.
K8,K2,F8,F2	DM0~3	**(Data Input/Output Mask)** DM controls data inputs.DM0 corresponds to the data on DQ0~DQ7.DM1 corresponds to the data on DQ8~DQ15……..
R8,P7,P8,N7,N8,M7, M8,L7,L3,M2,M3,N2, N3,P2,P3,R2,A8,B7, B8,C7,C8,D7,D8,E7, E3,D2,D3,C2,C3,B2, B3,A2	DQ0~31	**(Data Input/Output)** Data inputs and outputs are multiplexed on the same pin.
A9,F1,R9/ A1,F9,R1	V_{DD}/V_{SS}	**(Power Supply/Ground)** V_{DD} and V_{SS} are power supply pins for internal circuits.
A7,B1,C9,D1,E9,L9, M1,N9,P1,R7/A3,B9, C1,D9,E1,L1,M9,N1, P9,R3	V_{DDQ}/V_{SSQ}	**(Power Supply/Ground)** V_{DDQ} and V_{SSQ} are power supply pins for the output buffers.
F3,F7	NC/RFU	**(No Connection/Reserved for Future Use)** This pin is recommended to be left No Connection on the device.

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.5 ~ +2.3		V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.5 ~ +2.3		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +70	°C
		Extended	-25 ~ +85	
T_{STG}	Storage Temperature Range	-55 ~ +125		°C
P_D	Power Dissipation	1		W
I_{OS}	Short Circuit Current	50		mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (V_{CC}=1.8V± 0.1V, f=1MHz, T_A=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{CLK}	Clock Capacitance	1.5		4.0	pF
C_I	Input Capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	1.5		4.0	pF
C_O	Input/Output Capacitance	2.0		5.0	pF

Recommended DC Operating Conditions (T_A=0°C ~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.7	1.8	1.9	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	1.7	1.8	1.9	V
V_{IH}	Input Logic High Voltage	0.8* V_{DDQ}		V_{DDQ}+0.3	V
V_{IL}	Input Logic Low Voltage	-0.3		0.2*V_{DDQ}	V

Note: * All voltages referred to V_{SS}.

Recommended DC Operating Conditions

(V_{DD}=1.8V±0.1V, T_A=0°C ~ 70°C)

Symbol	Parameter	Test Conditions	Max.	Units
I_{DD1}	Operating Current *(Note 1)*	Burst length=2, t_{RC}εt_{RC}(min.), I_{OL}=0mA, One bank active	100	mA
I_{DD2P}	Precharge Standby Current in Power Down Mode	CKEδV_{IL}(max.), t_{CK}=min	1.5	mA
I_{DD2N}	Precharge Standby Current in Non-power Down Mode	CKEεV_{IL}(min.), t_{CK}=min, /CSεV_{IH}(min.) Input signals are changed one time during 2 clks	5	mA
I_{DD3P}	Active Standby Current in Power Down Mode	CKEδV_{IL}(max.), t_{CK}=min	3.5	mA
I_{DD3N}	Active Standby Current in Non-power Down Mode	CKEεV_{IH}(min.), t_{CK}=min, /CSεV_{IH}(min.) Input signals are changed one time during 2 clks	10	mA
I_{DD4}	Operating Current (Burst Mode) *(Note 2)*	t_{CK} ε t_{CK}(min.), I_{OL}=0mA, All banks active	170	mA
I_{DD5}	Refresh Current *(Note 3)*	t_{RC}ε t_{RFC} (min.), All banks active	110	mA
I_{DD6}	Self Refresh Current	CKEδ0.2V	1.4	mA

*All voltages referenced to V_{SS}.

Note 1: I_{DD1} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during t_{CK} (min.)

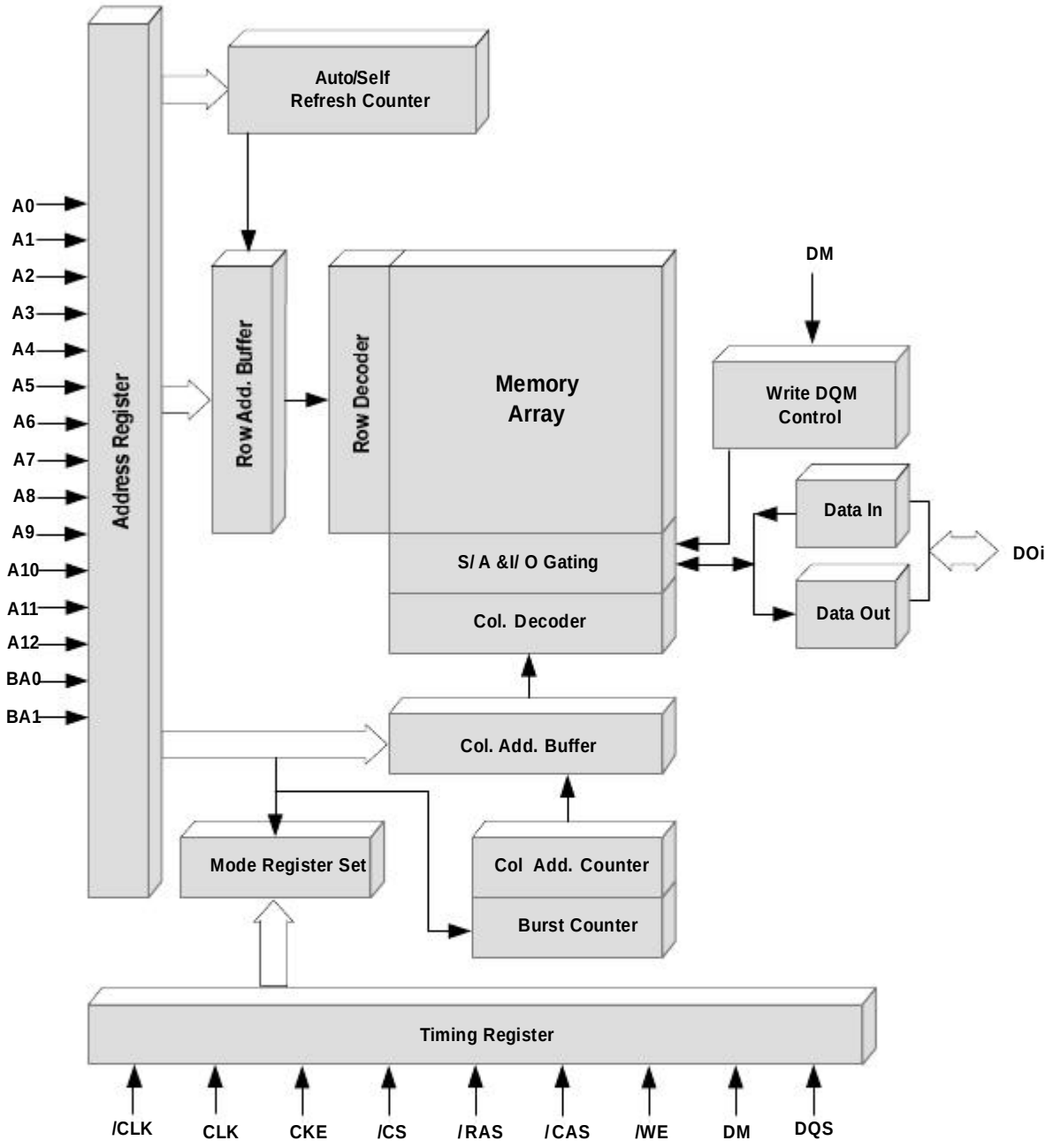
Note 2: I_{DD4} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during t_{CK} (min.)

Note 3: Min. of t_{RFC} (Auto refresh Row Cycle Times) is shown at AC Characteristics.

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input Leakage Current	0δV_IδV_{DDQ}, V_{DDQ}=V_{DD} All other pins not under test=0V	-2		+2	uA
I_{OL}	Output Leakage Current	0δV_OδV_{DDQ}, D_{OUT} is disabled	-1.5		+1.5	uA
V_{OH}	High Level Output Voltage	I_O=-0.1mA	0.9*V_{DDQ}			V
V_{OL}	Low Level Output Voltage	I_O=+0.1mA			0.1*V_{DDQ}	V

Block Diagram



AC Operating Conditions

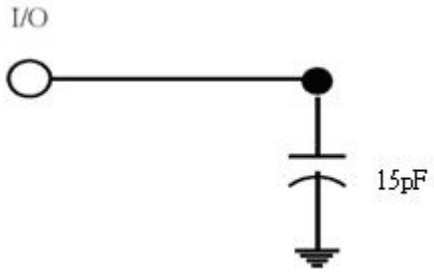
(V_{DD}=1.8V ± 0.1V, T_A=0°C ~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IX}	AC Input differential cross point voltage	0.4 × VDDQ	0.5 × VDDQ	0.6 × VDDQ	uA
V_{ID}	AC input differential voltage	0.6*V_{DDQ}		V_{DDQ}+0.6	uA
V_{OH}	High Level Output Voltage	0.8*V_{DDQ}		V_{DDQ}+0.3	V
V_{OL}	Low Level Output Voltage	-0.3		0.2*V_{DDQ}	V

Test Conditions

(V_{DD}=1.8V ± 0.1V, T_A=0°C ~70°C)

Item	Conditions
Input differential voltage, CK & /CK VID (AC)	1.4V
Output Load	See diagram as below
Input Signal Level	1.6V/0.2V
Transition Time of Input Signals	1V/ ns
Input differential cross point voltage,	0.5 × VDDQ



AC Operating Test Characteristics

(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

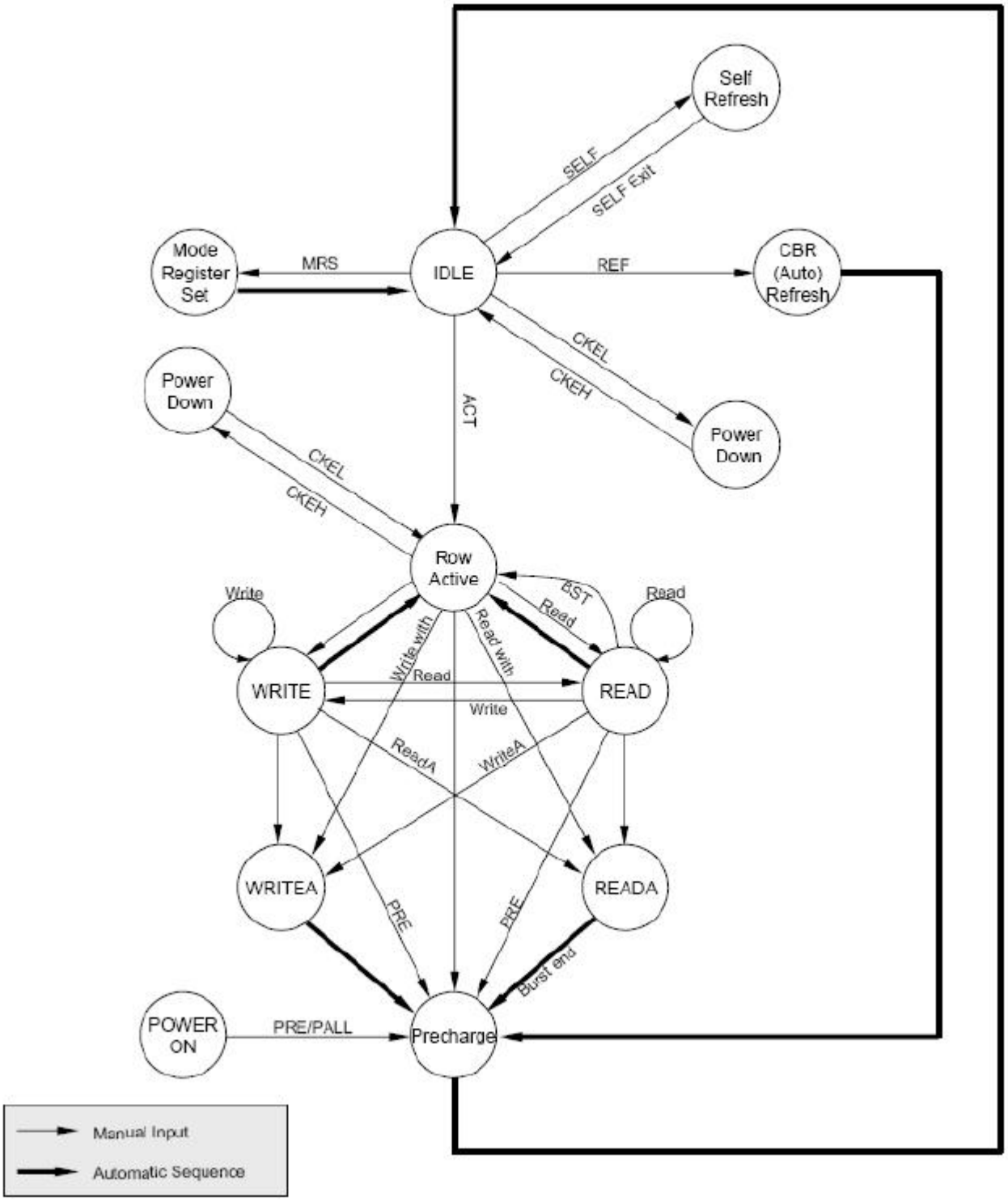
Symbol	Parameter	-6		-7.5		Units
		Min.	Max.	Min.	Max.	
t_{DQCK}	DQ output access from CLK,/CLK	2	5	2	6	ns
t_{DQSCK}	DQS output access from CLK,/CLK	2	5	2	6	ns
t_{CL},t_{CH}	CL low/high level width	0.45	0.55	0.45	0.55	t_{CK}
t_{CK}	Clock Cycle Time	6		7.5		ns
t_{DH},t_{DS}	DQ and DM hold/setup time	0.6		0.8		ns
t_{DIPW}	DQ and DM input pulse width for each input	1.75		1.75		ns
t_{HZ},t_{LZ}	Data out high/low impedance time from CLK,/CLK	1	5.5	1	6	ns
t_{DQSQ}	DQS-DQ skew for associated DQ signal		0.5		0.6	ns
t_{DQSS}	Write command to first latching DQS transition	0.75	1.25	0.75	1.25	t_{CK}
t_{DSL},t_{DSH}	DQS input valid window	0.35		0.35		t_{CK}
t_{MRD}	Mode Register Set command cycle time	2		2		t_{CK}
t_{WPRES}	Write Preamble setup time	0		0		ns
t_{WPRE}	Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	Write Postamble	0.4	0.6	0.4	0.6	t_{CK}
t_{IH},t_{IS}	Address/control input hold/setup time	1.1		1.3		ns
t_{RPRE}	Read Preamble	0.9	1.1	0.9	1.1	t_{CK}

AC Operating Test Characteristics (Continued)

(V_{DD}=1.8V±0.1V, T_A=0°C ~70°C)

Symbol	Parameter	-6		-75		Units
		Min.	Max.	Min.	Max.	
t_{RPST}	Read Postamble	0.4	0.6	0.4	0.6	t_{CK}
t_{RAS}	Active to Precharge command period	42	120k	45	120k	ns
t_{RC}	Active to Active command period	60		75		ns
t_{RFC}	Auto Refresh Row Cycle Time	138		138		ns
t_{RCD}	Active to Read or Write delay	30		30		ns
t_{RP}	Precharge command period	22.5		22.5		ns
t_{RRD}	Active bank A to B command period	12		15		ns
t_{CCD}	Column address to column address delay	1		1		t_{CK}
t_{CDLR}	Last data in to Read command	2.5 t_{CK}- t_{DQSS}		2.5 t_{CK}- t_{DQSS}		t_{CK}
t_{HZP}	Pre-charge command to high-Z	3		3		t_{CK}
t_{CDLW}	Last data in to Write command	1		1		t_{CK}
t_{DPL}	Last data in to Precharge command	3		3		t_{CK}
t_{WTR}	Internal Write to Read command delay	2		1		t_{CK}
t_{CKE}	CKE minimum pulse width	2		2		t_{CK}
t_{WPD}	Write to pre-charge delay(same bank)	4+ BL/2		3+ BL/2		t_{CK}
t_{RPD}	Read to pre-charge delay(same bank)	BL/2		BL/2		t_{CK}
t_{WRD}	Write to Read command delay	3+ BL/2		2+ BL/2		t_{CK}
t_{BSTW}	Burst stop to write delay	3		3		t_{CK}
t_{WR}	Write recovery	15		15		ns
t_{XSNR}	Exit self Refresh to non-read command	120		120		ns
t_{XSRD}	Exit self Refresh to read command	200		200		ns
t_{REFI}	Average periodic refresh interval		7.8		7.8	us

Simplified State Diagram



1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A12~A0
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	L	H	H	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power Down Entry		H	L	X	X	X	X	X
Power Down	Power Down Exit		L	H	X	X	X	X	X

Remark H = High level, L = Low level, X = High or Low level (Don't care)

3. Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT/BW	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	Bank active,Latch RA
	L	L	H	L	BA, A10	PRE/PREA	NOP*(Note 3)*
	L	L	L	H	X	REFA	Auto refresh*(Note 4)*
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode register
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA/CA/A10	READ/READA	Begin read,Latch CA, Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write,Latch CA, Determine auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	Precharge/Precharge all
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	Terminal burst
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst,Latch CA, Begin new read, Determine Auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst, PrecharE
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst with DM="H",Latch CA,Begin read,Determine auto-precharge *(Note 2)*
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst,Latch CA,Begin new write, Determine auto-precharge *(Note 2)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst with DM="H", Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	BA/CA/A10	TERM	ILLEGAL
	L	H	L	X	BA/RA	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/A10	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	X	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP}) *(Note 3)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	NOP(Row active after t_{RCD})
	L	H	H	H	X	NOP	NOP(Row active after t_{RCD})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL *(Note 1)*
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA/CA/A10	READ	ILLEGAL *(Note 1)*
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP
	L	L	H	H	BA/RA	ACT	ILLEGAL *(Note 1)*
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL *(Note 1)*
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 1: ILLEGAL to bank in specified states;
Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 2: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 3: NOP to bank precharging or in idle state.May precharge bank indicated by BA.

Note 4: ILLEGAL of any bank is not idle.

4. Command Truth Table for CKE

Current State	CKE n-1	CKE n	/CS	/R	/C	/W	Addr.	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Self-Refresh
	L	H	L	H	H	H	X	Exist Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain self refresh)
Both bank precharge power down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Power down
	L	H	L	H	H	H	X	Exist Power down
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power down)
All Banks Idle	H	H	X	X	X	X	X	Refer to function true table
	H	L	H	X	X	X	X	Enter power down mode *(Note 3)*
	H	L	L	H	H	H	X	Enter power down mode *(Note 3)*
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row active/Bank active
	H	L	L	L	L	H	X	Enter self-refresh *(Note 3)*
	H	L	L	L	L	L	Op-Code	Mode register access
	H	L	L	L	L	L	Op-Code	Special mode register access
	L	X	X	X	X	X	X	Refer to current state
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to command truth table

Remark: H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1: After CKE's low to high transition to exist self refresh mode.And a time of t_{RC}(min) has to be Elapse after CKE's low to high transition to issue a new command.

Notes 2:CKE low to high transition is asynchronous as if restarts internal clock.

Notes 3:Power down and self refresh can be entered only from the idle state of all banks.

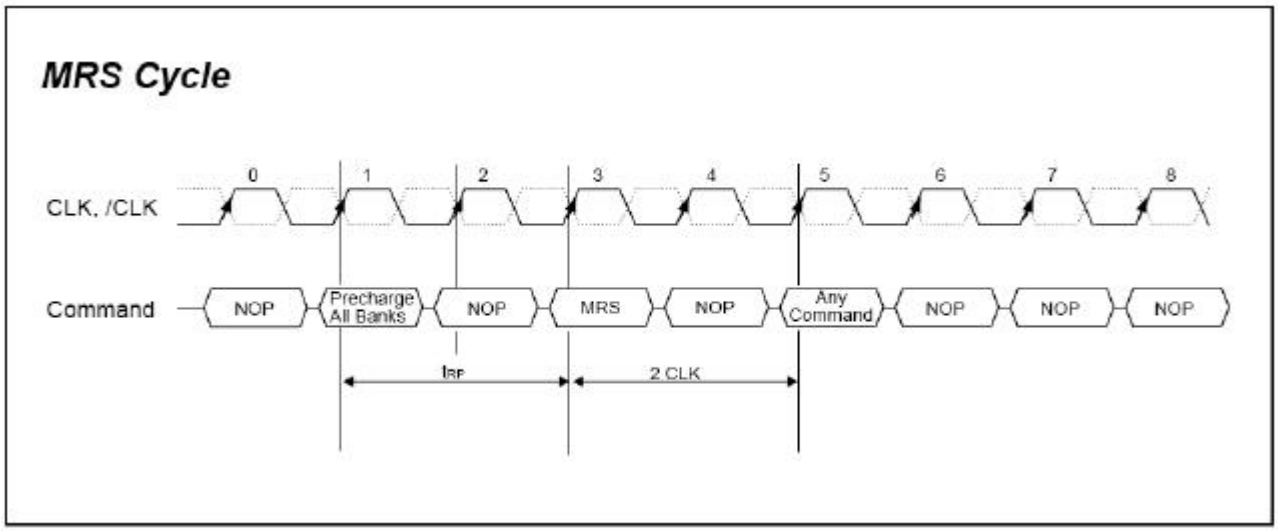
Recommended Power On and Initialization

The following power on and initialization sequence guarantees the device is preconditioned to each user's specific needs.
Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level..
Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.
After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command.
Provide NOPs or DESL commands for at least tRP time.
Issue an auto-refresh command followed by NOPs or DESL command for at least tRFC time. Issue the second auto-refresh command followed by NOPs or DESL command for at least tRFC time.
Note as part of the initialization sequence there must be two auto-refresh commands issued.
Using the MRS command, load the base mode register. Set the desired operating modes.
Provide NOPs or DESL commands for at least tMRD time.
Using the MRS command, program the extended mode register for the desired operating modes.
Provide NOP or DESL commands for at least tMRD time.
Now it is ready for any valid command.

Mode Register Definition

Mode Register Set

The mode register stores the data for controlling the various operating modes of DDR SDRAM which contains addressing mode, burst length, /CAS latency, test mode, DLL reset and various vendor ' s specific opinions. The defaults values of the register is not defined, so the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register.) The state of the address pins A0-A12 in the same cycle as /CS, /RAS, /CAS, /WE and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operating as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, addressing mode uses A3, /CAS latency (read latency from column address) uses A4-A6. A7 is used for test mode. A8 is used for DDR reset. A7 must be set to low for normal MRS operation.



Address input for Mode Register Set

BA1	BA0	A12/11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU							CAS Latency			BT	Burst Length		

BA0	An – A0
0	MRS Cycle
1	EMRS

Burst Length				
Sequential	Interleave	A2	A1	A0
Reserved	Reserved	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
16	16	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Reserved	Reserved	1	1	1

Burst Type	A3
Sequential	0
Interleave	1

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
Reserved	0	1	0
3	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Burst Type (A3)

Burst Length	A3	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	X	0	01	01
	X	X	X	1	10	10
4	X	X	0	0	0123	0123
	X	X	0	1	1230	1032
	X	X	1	0	2301	2301
	X	X	1	1	3012	3210
8	X	0	0	0	01234567	01234567
	X	0	0	1	12345670	10325476
	X	0	1	0	23456701	23016745
	X	0	1	1	34567012	32107654
	X	1	0	0	45670123	45670123
	X	1	0	1	56701234	54761032
	X	1	1	0	67012345	67452301
	X	1	1	1	70123456	76543210
16	0	0	0	0	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
	0	0	0	1	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0	1 0 3 2 5 4 7 6 9 8 11 10 13 12 15 14
	0	0	1	0	2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1	2 3 0 1 6 7 4 5 10 11 8 9 14 15 12 13
	0	0	1	1	3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2	3 2 1 0 7 6 5 4 11 10 9 8 15 14 13 12
	0	1	0	0	4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3	4 5 6 7 0 1 2 3 12 13 14 15 8 9 10 11
	0	1	0	1	5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4	5 4 7 6 1 0 3 2 13 12 15 14 9 8 11 10
	0	1	1	0	6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5	6 7 4 5 2 3 0 1 14 15 12 13 10 11 8 9
	0	1	1	1	7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8
	1	0	0	0	8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7
	1	0	0	1	9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8	9 8 11 10 13 12 15 14 1 0 3 2 5 4 7 6
	1	0	1	0	10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9	10 11 8 9 14 15 12 13 2 3 0 1 6 7 4 5
	1	0	1	1	11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10	11 10 9 8 15 14 13 12 3 2 1 0 7 6 5 4
	1	1	0	0	12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11	12 13 14 15 8 9 10 11 4 5 6 7 0 1 2 3
	1	1	0	1	13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12	13 12 15 14 9 8 11 10 5 4 7 6 1 0 3 2
	1	1	1	0	14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13	14 15 12 13 10 11 8 9 6 7 4 5 2 3 0 1
	1	1	1	1	15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

* Page length is a function of I/O organization and column addressing

Extended Mode Register Set (EMRS)

The Extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA1 (The DDR SDRAM should be in all bank precharge with CKE already prior to writing into the extended mode register.) The state of address pins A0-A10 and BA1 in the same cycle as /CS, /RAS, /CAS, and /WE going low is written in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. High on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation.

BA1	BA0	A12/11/10	A9	A7	A6/5	A4/3	A2/1/0
1		0	ATCSR	0	DS	0	PASR

A9	ATCSR
0	Enable
1	R

BA0	An – A0
0	MRS Cycle
1	EMRS

Driver Strength	A6	A5
Normal	0	0
1/2 strength	0	1
1/4 strength	1	0
1/8 strength	1	1

Partial Array Self Refresh Refresh Array	A2	A1	A0
All banks	0	0	0
Bank A & B (BA1=0)	0	0	1
Bank A (BA0=BA1=0)	0	1	0
R	0	1	1
R	1	0	0
R	1	0	1
R	1	1	0
R	1	1	1

Output Drive Strength

The normal drive strength got all outputs is specified to be LV-CMOS. By setting EMRS specific parameter on A6 and A5, driving capability of data output drivers is selected.

Temperature Compensated Self-Refresh

TCSR controlled by programming in the extended mode register (EMRS). The memory automatically changes the self-refresh cycle by temperature fluctuations.

Partial Array Self Refresh

In EMRS setting ,memory array size to be refreshed during self-refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self-refresh.

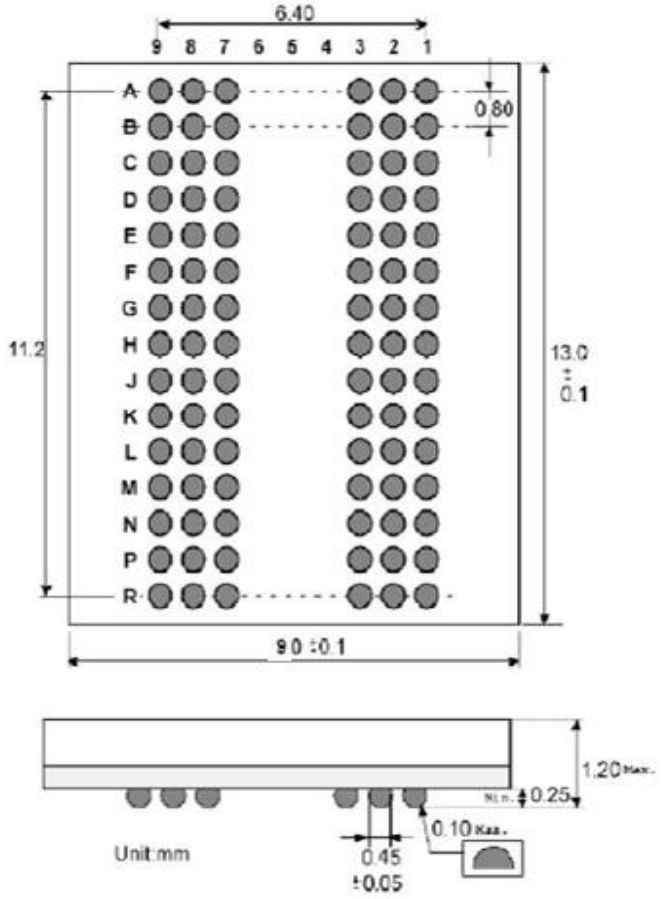
Package Description

90-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

nm



±0.05